#### WEST

# Freeform Search

| Database:             | US Patents Full-Text Database US Pre-Grant Publication Full-Text Database JPO Abstracts Database EPO Abstracts Database Derwent World Patents Index IBM Technical Disclosure Bulletins |
|-----------------------|--|
| Term:                 |  |
| Display:<br>Generate: | Documents in Display Format: TI Starting with Number 1  Hit List Hit Count Side by Side Image  |
|                       | Search Clear Help Logout Interrupt   |
|                       | Main Menu Show S Numbers Edit S Numbers Preferences Cases  |

#### **Search History**

DATE: Friday, May 02, 2003 Printable Copy Create Case

| Set Name<br>side by side  |   | Hit Count | Set Name<br>result set |
|---------------------------|---|-----------|------------------------|
| DB=USPT; PLUR=YES; OP=ADJ |   |           |                        |
| <u>L9</u>                 | L6 and (code near4 execut\$4)   | 11        | <u>L9</u>              |
| <u>L8</u>                 | L7 and ((RAM or SRAM or DRAM or volatile) near8 code)                               | 2         | <u>L8</u>              |
| <u>L7</u>                 | L6 and (flash near8 (modular or (single adj die) or (single adj chip) or embedded)) | 20        | <u>L7</u>              |
| <u>L6</u>                 | NAND near3 flash  | 681       | <u>L6</u>              |
| <u>L5</u>                 | L4 and (code near8 boot\$4)   | 37        | <u>L5</u>              |
| <u>L4</u>                 | L3 and 12   | 73        | <u>L4</u>              |
| <u>L3</u>                 | (RAM or SRAM or DRAM or volatile) near8 ((portion or section or part) near4 code)   | 512       | <u>L3</u>              |
| <u>L2</u>                 | L1 near8 code near4 execut\$4   | 1410      | <u>L2</u>              |
| <u>L1</u>                 | (flash or (non adj volatile) or ROM)  | 241555    | <u>L1</u>              |

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DATE: Friday, May 02, 2003 Printable Copy Create Case

| Set Name Query side by side |  | Hit Count | Set Name result set |
|-----------------------------|--|-----------|---------------------|
| DB=USPT; PLUR=YES; OP=ADJ   |  |           |                     |
| <u>L8</u>                   | L6 and (flash with \$2RAM with (die or chip or embedded))  | 13        | <u>L8</u>           |
| <u>L7</u>                   | L6 and ((711/\$)!.CCLS.)   | 13        | <u>L7</u>           |
| <u>L6</u>                   | L5 and ((power or current or voltage) near8 (\$4ROM or flash or (non adj volatile)))                       | 110       | <u>L6</u>           |
| <u>L5</u>                   | L4 and ((\$4ROM or flash) near8 (code or instruction) near8 (stor\$3 or receiv\$4))                        | 173       | <u>L5</u>           |
| <u>L4</u>                   | L3 and boot\$4   | 228       | <u>L4</u>           |
| <u>L3</u>                   | L2 and ((host or CPU or processor) near8 ((code or instruction) near4 execut\$4))                          | 668       | <u>L3</u>           |
| <u>L2</u>                   | L1 and ((RAM or (random adj access adj memory) or volatile) near8 ((code or instruction) near4 execut\$4)) | 1094      | <u>L2</u>           |
| <u>L1</u>                   | (\$4ROM or flash) near8 ((code or instruction) near4 execut\$4)  | 4027      | <u>L1</u>           |